REMARKS

The invention centers on the idea of performing a comparison of steady state DC conditions corresponding to the beginning and end of a test cycle (present claim 1 step (c)) and storing such information (present claim 1 step (d)) prior to performing any testing/simulation of transient response (present claim 8 step (f) and present claim 14, step (f)). In this manner, adjustments can be made either to the test conditions and/or to the device configuration prior to starting computation-intensive transient response analysis.

Joshi et al. (US6442735) discloses an SOI circuit simulation method where "DC analysis" is performed prior to transient response simulation. The DC analysis of Joshi et al. appears to be an assessment relative to an initial DC condition. Joshi et al. does not disclose or suggest comparing device response to two different DC conditions as in present claim 1 step (c), nor storing any information based on such a comparison as in present claim 1 step (d). Joshi et al. does not disclose or suggest performing transient analysis after such comparison of DC conditions as in claim 8 step (f) and claim 14, step (f).

Dangello et al. (US 5555201) discloses techniques and systems for hierarchical display of control and dataflow information. Dangello et al. appears to be relied on for its disclosure concerning object-oriented displays. Dangello et al. does not disclose or suggest anything regarding DC testing, much less comparing device response to two different DC conditions and storing any information based on such a comparison.

Applicants submit that the above arguments for patentability do not rely on unclaimed features. Thus, applicants submit that the present claims do not represent obviousness-type double patenting over Joshi et al. in view of

Dangelo et al. For the above reasons, applicants further submit that the claims are not anticipated by Joshi et al.

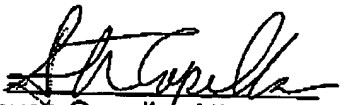
Wong (US Patent 4,918,643) describes a method of developing a linear vector description of system response over a cycle where the system is to be forced to steady state. Where the series of vectors does not result in a steady state at the end of the cycle, Wong changes the initial vector using a Jacobian matrix calculation. Since this method potentially involves multiple Jacobian matrix calculations, Wong describes an alternative method for computing the Jacobian matrix. Wong compares the starting vector with the final vector to see if final vector is substantially the same as the starting vector. This final vector is the result of a transient calculation using the series of linear vectors described in Wong. Wong does not do a DC simulation of end of cycle conditions as required by the present claims. Applicants submit that Wong does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop. Wong does not disclose or suggest performing transient analysis after manual correction as required by present claims 8 and 14.

Wong et al. (IEEE article) discloses a method of switching regulator analysis where the an open loop configuration is used to lessen the impact of the feedback circuitry in the case of a poor guess. Wong et al. performs a time domain simulation technique assuming a periodic network waveform and then iteratively runs the simulation until starting conditions are found which result in a steady state condition. Wong et al. does not do a DC simulation of end of cycle conditions as required by the present claims. Applicants submit that Wong et al. does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop. Wong et al. does not disclose or suggest performing transient analysis after manual correction as required by present claims 8 and 14.

Sakamoto (US6063130) appears to employ a passivity check for linear circuit elements prior to transient response simulation. Sakamoto performs this passivity check by preparing and inductance matrix and checking the minor determinants. If the element is not passive, this result is reported back and the testing is aborted. Sakamoto does not give any apparent details regarding the DC analysis of figure 2, step 24. At best, this would appear to be a DC analysis of the cycle start condition. Sakamoto does not disclose or suggest comparing device response to two different DC conditions, nor storing any information based on such a comparison. Sakamoto does not disclose or suggest performing corrections based on such comparison of conditions prior to transient analysis. The combination of Sakamoto with the teaching of Wong or Wong et al. would not render the invention obvious in as much as the combined teaching of these references would not lead one of ordinary skilled in the art to perform the comparison of DC simulations and/or manual correction prior to transient analysis in response to such comparison as presently claimed.

For the above reasons, applicants submit that the claims are patentable over the prior art of record and that the application is in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,
Karl-Eugen Kroell et al.

By 
Steven Capella, Attorney
Reg. No. 33,086
Telephone: 845-894-3669